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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/933,166	Applicant(s) Sano et al.
	Examiner Wilson Lee	Art Unit 2821

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Aug 27, 2003*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-33, 35, and 37-98* is/are pending in the application.

4a) Of the above, claim(s) *41-62* is/are withdrawn from consideration.

5) ☒ Claim(s) *33, 63, and 64* is/are allowed.

6) ☒ Claim(s) *1-29, 32, 35, 37-40, 65-71, 73-83, 86, 87, 90, 93, and 96* is/are rejected.

7) ☒ Claim(s) *30, 31, 72, 84, 85, 88, 89, 91, 92, 94, 95, 97, and 98* is/are objected to.

8) ☒ Claims *41-62* are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Remarks

Applicant's arguments filed on 8/27/03 have been fully considered but they are not persuasive.

In regard to Claims 1, 9, 17 and 71:

Applicant asserts that Katayama discloses two power distributing circuits in lieu of one power distributing circuit as claimed and fails to disclose the claimed limitation "without providing another power distributing circuit between a reference potential point and the driving device" and "without providing another power distributing circuit between a driving power supply source and the driving device".

Examiner respectfully disagrees.

Katayama clearly discloses only one single power distributing circuit comprising MOSFETs 10, 11 and a controller (See Col. 3, lines 50-51). These three elements function as a power distributing circuit for distributing power from the source to the device. Katayama does not have another power distributing circuit connected elsewhere in his invention. Thus, there is no another power distributing circuit, such that Katayama meets the newly added limitations in claims 1, 9, 17, 71. It is noted that Katayama's power source (9) supplying positive voltage from plus terminal to MOSFET (10) and negative voltage from minus terminal to MOSFET (11) (See Figure 1).

In regard to Claims 35, 65 and 68:

Applicant argues that Katayama fails to disclose that the power distributing circuit (comprised of resistors 12, 13) is a resistive element having an impedance whose value is not smaller than one-tenth of the value of a resistive component of a conducting

impedance of a driving device because the resistors (12, 13) of Katayama must be low values so as to apply the high voltage at high speed (alleged by applicant).

Examiner respectfully disagrees.

Merely interpreted from applicant's explanation, in order to apply high voltage, Katayama's resistors (12, 13) must be very high instead because according to Ohm's law, V=iR, voltage is equal to current x resistance. Therefore, resistance of Katayama's resistors (12, 13) must be very high in order to apply high voltage. Besides, the amount of current or voltage from power source (9) does not affect the speed of the circuit. Power source just merely plays a role of a power supplier. The speed of the circuit is affected by input signal to the gate, not by the source of a transistor or MOSFET.

In addition, as explained in the previous office action, resistance of Katayama must be very high because power source (9) is a high voltage source. The circuit needs high resistive element to regulate high voltage, which is applied to the loads. If the resistance (12, 13) is very low in Katayama (See Figure 3) as alleged by applicant, there is no need to place any resistors between the power source and the load in Katayama. Why not just connect two conductive wires (it means very low resistance or even not resistive) directly to the circuit (5) from the power source (9), which totally ignore the resistors? Thus, the resistance of the resistors (12, 13) cannot be very low.

In regard to Claims 66 and 69:

Applicant argues that Katayama fails to disclose a constant current source.

Examiner respectfully disagrees.

Katayama's power distributing circuit (resistors 12, 13) is not variable (See Figure 3). Therefore, the current flows through the resistor will be unchanged since the resistance of resistors (12, 13) does not change.

In addition, the power distributing circuit (10 and 11, or 12 and 13) is constantly supplying current to the circuit (5) until the switches are off.

In regard to Claims 67 and 70:

Applicant argues that Katayama fails to disclose that the input withstand voltage is higher than an output voltage because the withstand voltage of LDMOS is not increased (alleged by applicant).

Examiner respectfully disagrees.

No matter the withstand voltage is increased or not, it is still inherently higher than the output voltage. As explained in the previous office, Katayama discloses that the driving device (5) has high voltage endurance (See Col. 4, lines 10-11). Since his driving device (5) is intentionally designed to endure high voltage or in other word, hold high voltage or receive high voltage, thus the input withstand voltage must be very high so that the designed high voltage endurable driving device (5) can endure this high voltage input. In addition, the load is comprised of EL element, which are fragile elements. The output voltage to the EL element cannot be very high otherwise the load would be blown up or burned.

In regard to the argument based on Miyazaki reference:

Applicant argues that each of driving devices (amplifiers) A1 to A5 does receive electric power from a plurality of voltage (VI1 to VI5) and none of resistors R1 to R5 distribute electric power from the driving devices A1 to A5.

Examiner respectfully disagrees.

Miyazaki clearly discloses that the amplifier (A1) receives power from VI1, amplifier (A2) from VI2, etc. And resistors (R1 to R5) distribute power to the amplifiers (See Figure 2). It is noted that the alleged limitation "resistors distribute electric power from the driving devices" is not recited in any claim of the instant application.

Claim Rejections – 35 U.S.C. 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-9, 12-18, 21-25, 28, 29, 32, 65-71, 73-79, 82, 83, 86 are rejected under 35 U.S.C. 102(e) as being anticipated by Katayama et al. (6,556,177).

Regarding Claim 1, Katayama discloses a capacitive load (4) driving circuit comprising:

- a driving device (5) connecting a driving power supply source (9) to an output terminal (5a) connectable to a capacitive load (4); and

- a power distributing circuit (12 and 13, or 10 and 11) connected between the driving power supply source (9) and the driving device (5) (See Figure 3) without providing another power distributing circuit between a reference potential point and the driving device.

Regarding Claim 4, Katayama discloses that the power distributing circuit is inherently a constant-current source since it renders unchanged current directly from the power source (9).

Regarding Claim 5, Katayama discloses that the driving power supply source (9) outputs a plurality of different voltage levels in a selective manner controlled by the power transistors (10 and 11) such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 6, Katayama discloses that the power distributing circuit includes a plurality of power distributing units (power transistors 10 and 11), one for each of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 7, Katayama discloses that each of the power distributing units (10 and 11) has a function as a switch for selecting one of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 8, Katayama discloses that the driving device (5) is a device whose input withstand voltage is inherently higher than an output voltage since Katayama discloses the driving device (5) has high voltage endurance (See Col. 4, lines 10-11) so that it can withstand high voltage and the output voltage is lowered in order to prevent blowing up the voltage sensitive loads.

Regarding Claim 9, Katayama discloses a capacitive load driving circuit comprising: a driving device comprising a reference potential (terminals +, -) of the power source (9) to an output terminal (5a); and a power distributing circuit (12 and 13) connected between the reference potential point (terminals +, -) and the driving device (5) without providing another power distributing circuit between a driving power supply source and the driving device (See Figure 3).

Regarding Claim 12, Katayama discloses that the power distributing circuit is inherently a constant-current source since it renders unchanged current directly from the power source (9).

Regarding Claim 13, Katayama discloses that the driving power supply source (9) outputs a plurality of different voltage levels in a selective manner controlled by the power transistors (10 and 11) such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 14, Katayama discloses that the power distributing circuit includes a plurality of power distributing units (power transistors 10 and 11), one for each of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 15, Katayama discloses that each of the power distributing units (10 and 11) has a function as a switch for selecting one of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claims16, Katayama discloses that the driving device (5) is a device whose input withstand voltage is inherently higher than an output voltage since Katayama discloses the driving device (5) has high voltage endurance (See Col. 4, lines

10-11) so that it can withstand high voltage and the output voltage is lowered in order to prevent blowing up the voltage sensitive loads.

Regarding Claims 17, 71, Katayama discloses a capacitive load driving circuit comprising:

- a plurality of driving devices (6) driving a plurality of capacitive loads (4) and formed in integrated-circuit form (See abstract); and
- a power distributing circuit (15, or 12 & 13, or 10 & 11) connected between each of the plurality of driving devices (6) to a driving power supply source (9) or to a reference potential point (+, -) without providing another power distributing circuit between each of the plurality of driving devices and a reference potential point (See Figures 1, 3 or 4).

Regarding Claim 18, Katayama discloses that a diode (shown in Figure 5A) inserted between each of the capacitive loads (4) and a corresponding one driving devices (6) (See Figure 6).

Regarding Claim 21, Katayama discloses that the power distributing circuit (12 & 13) is inherently a constant-current source since it renders unchanged current directly from the power source (9).

Regarding Claim 22, Katayama discloses that the driving power supply source (9) outputs a plurality of different voltage levels in a selective manner controlled by the power transistors (10 and 11) such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 23, Katayama discloses that the power distributing circuit includes a plurality of power distributing units (power transistors 10 and 11), one for

each of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 24, Katayama discloses that each of the power distributing units (10 and 11) has a function as a switch for selecting one of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 25, Katayama discloses that the driving device (5) is a device whose input withstand voltage is inherently higher than an output voltage since Katayama discloses the driving device (5) has high voltage endurance (See Col. 4, lines 10-11) so that it can withstand high voltage and the output voltage is lowered in order to prevent blowing up the voltage sensitive loads.

Regarding Claim 28, Katayama discloses that a series connection (5b) of each of the power distributing circuit (15) and a switch device (10) is provided between each of the driving devices (6) and the driving power supply source (9) (See Figures 1 and 4).

Regarding Claim 29, Katayama discloses that the capacitive load driving circuit is constructed as a driving module (5) containing a plurality of driving integrated circuits (6) for driving the capacitive loads (4) (See Figure 1).

Regarding Claim 32, Katayama discloses a switch device (10 or 11) inserted between the power distributing circuit (15) and the driving power supply source (9) and the switching being caused to conduct after the driving devices (7) have been switched into a conducting state (See Figure 5B. Switch device is in conductive state when driving device (7) is also in conductive state).

Regarding Claim 65, as discussed above in details in the preceding rejections of claims 1 and 2, Katayama meets the limitation of claim 65.

Regarding Claim 66, as discussed above in details in the preceding rejections of claims 1 and 4, Katayama meets the limitation of claim 66.

Regarding Claim 67, as discussed above in details in the preceding rejections of claims 1 and 8, Katayama meets the limitation of claim 67.

Regarding Claim 68, as discussed above in details in the preceding rejections of claims 9 and 10, Katayama meets the limitation of claim 68.

Regarding Claim 69, as discussed above in details in the preceding rejections of claims 9 and 12, Katayama meets the limitation of claim 69.

Regarding Claim 70, as discussed above in details in the preceding rejections of claims 9 and 16, Katayama meets the limitation of claim 70.

Regarding Claim 73, Katayama discloses that the driving device (5) is a device whose input withstand voltage is inherently higher than an output voltage since Katayama discloses the driving device (5) has high voltage endurance (See Col. 4, lines 10-11) so that it can withstand high voltage and the output voltage is lowered in order to prevent blowing up the voltage sensitive loads.

Regarding Claim 74, Katayama discloses that each of the power distributing circuits (12, 13) is an inherent high power resistor having a capability of handle power higher than the allowable power of the driving device since resistors (12, 13) must be highly resistive in order to regulate high voltage from high AC source to the fragile loads.

Regarding Claim 75, Katayama discloses that the power distributing circuit is inherently a constant-current source since it renders unchanged current directly from the power source (9).

Regarding Claim 76, Katayama discloses that the driving power supply source (9) outputs a plurality of different voltage levels in a selective manner controlled by the power transistors (10 and 11) such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 77, Katayama discloses that the power distributing circuit includes a plurality of power distributing units (power transistors 10 and 11), one for each of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 78, Katayama discloses that each of the power distributing units (10 and 11) has a function as a switch for selecting one of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 79, Katayama discloses that the driving device (5) is a device whose input withstand voltage is inherently higher than an output voltage since Katayama discloses the driving device (5) has high voltage endurance (See Col. 4, lines 10-11) so that it can withstand high voltage and the output voltage is lowered in order to prevent blowing up the voltage sensitive loads.

Regarding Claim 82, Katayama discloses that a series connection (5b) of each of the power distributing circuit (15) and a switch device (10) is provided between each of the driving devices (6) and the driving power supply source (9) (See Figures 1 and 4).

Regarding Claim 83, Katayama discloses that the capacitive load driving circuit is constructed as a driving module (5) containing a plurality of driving integrated circuits (6) for driving the capacitive loads (4) (See Figure 1).

Regarding Claim 86, Katayama discloses a switch device (10 or 11) inserted between the power distributing circuit (15) and the driving power supply source (9) and the switching being caused to conduct after the driving devices (7) have been switched into a conducting state (See Figure 5B. Switch device is in conductive state when driving device (7) is also in conductive state).

Claims 1, 9, 17, 26, 27, 33, 35, 38-40, 71, 80 and 81 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyazaki (6,501,467).

Regarding Claim 1, Miyazaki discloses a capacitive load driving circuit comprising:

- a driving device (A1-A5) connecting a driving power supply source (VI1) to an output terminal (V1-V5) connectable to a capacitive load (C1); and
- a power distributing circuit (R1-R5) connected between the driving power supply source (VI1) and the driving device (A1-A5) (See Figure 3).

Regarding Claim 9, Miyazaki discloses a capacitive load driving circuit comprising:

- a driving device (A1-A5) connecting a reference potential point (VI2-VI5) to an output terminal (upper terminal of C1, or V1-V5);
- a power distributing circuit (R1-R5) inserted between the reference potential point (VI2-VI5) and the driving device (A1-A5) (See Figure 2).

Regarding Claims 17 and 71, Miyazaki discloses a capacitive load driving circuit comprising:

- a plurality of driving devices (A1-A5) driving a plurality of capacitive loads (C1-C5) and inherently formed in integrated-circuit form since it is a compact display panel; and
- a power distributing circuit (R1-R5) connecting each of the plurality of driving devices (A1-A5) to a driving power supply source (VI1) or to a reference potential point (VI2-VI5).

Regarding Claim 26, Miyazaki discloses that a ground terminal (ground terminal is shown on the right bottom nearby VEE) of each of the integrated driving devices (A1-A5) is connected to the driving power supply source (VI1) via the power distributing circuit (R1-R5) (See Figure 2).

Regarding Claim 27, Miyazaki discloses that a ground terminal terminal (ground terminal is shown on the right bottom nearby VEE) of each of the integrated driving devices (A1-A5) is connected to the reference potential point (VI2-VI5) via the power distributing circuit (R1-R5) (See Figure 2).

Regarding Claim 33, Miyazaki discloses a capacitive load driving circuit including a configuration in which a driving power supply source (VI1-VI5 or VEE) is connected to an output terminal (V1-V5) via a driving device (A1-A5), wherein the driving power supply source (VI1-VI5 or VEE) outputs a plurality of different voltage levels in a selective manner (See Figures 3 and 11 and Col. 6, lines 38-56).

Regarding Claim 35, Miyazaki discloses a capacitive load driving circuit for driving a capacitive load (C1-C5), connected to an output terminal, by a driving device (A1-A5), comprising a resistive impedance (R1-R5) inserted in series to the output terminal (V1-V5) (See Figures 2 or 3).

Regarding Claim 38, Miyazaki discloses that a driving power supply source (VI1) connected to the output terminal (V1-V5) via the driving device (A1-A5); and a power distributing circuit (R1-R5) inserted between the driving power supply source (9) and the driving device (A1-A5) (See Figure 2).

Regarding Claim 39, Miyazaki discloses that a reference potential point (VI2-VI5) connected to the output terminal (VI-V5) via the driving device (A1-A5); and a power distributing circuit (R1-R5) inserted between the reference potential point (VI2-VI5) and the driving device (A1-A5) (See Figure 2).

Regarding Claim 40, Miyazaki discloses that a plurality of driving devices (A1-A5) for driving a plurality of capacitive loads (C1-C5), inherently formed in integrated-circuit form, wherein each of the driving devices is connected to a driving power supply source (VI1) or a reference potential point (VI2-VI5) via a power distributing circuit (R1-R5) (See Figure 2).

Regarding Claim 80, Miyazaki discloses that a ground terminal (see Figures 1 and 2) of each of the integrated driving devices (A1 to A5) is connected to the driving power supply source (VI1) via the power distributing circuit (R1-R5).

Regarding Claim 81, Miyazaki discloses that the ground terminal of each of the integrated driving devices (A1-A5) is connected to the reference potential point (VI2-VI5) via the power distributing circuits (R1-R5) (See Figures 1 and 2).

Claim Rejections – 35 U.S.C. 102/103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 10, 11, 19, 20, 36, 37, 87, 90, 93 and 96 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Katayama et al. (6,556,177).

Regarding Claim 2, Katayama discloses that the power distributing circuit (12 and 13) is a resistive element having an impedance whose value is inherently not small than 1/10 of the value of a resistive component of the conducting impedance of the driving device (5) since the resistors (12 and 13) must be particularly high in order to regulate the high voltage from the AC source (9) and the resistive component inside the transistors (6, 7, 8) of driving device (5) are driven with small gate current (See Col. 4, lines 10-13) and 1/10 of the value of the resistive component in the driving device is intended to be very small.

Regarding Claim 3, Katayama discloses that the power distributing circuit (12 and 13) is inherently a high-power resistor having a capability to handle power higher

than the allowable power of the driving device in order to regulate the high voltage from the AC source to the transistors (6, 7, 8) of the driving device (5).

Regarding Claim 10, Katayama discloses that the power distributing circuit (12 and 13) is a resistive element having an impedance whose value is inherently not small than 1/10 of the value of a resistive component of the conducting impedance of the driving device (5) since the resistors (12 and 13) must be particularly high in order to regulate the high voltage from the AC source (9) and the resistive component inside the transistors (6, 7, 8) of driving device (5) are driven with small gate current (See Col. 4, lines 10-13) and 1/10 of the value of the resistive component in the driving device is intended to be very small.

Regarding Claim 11, Katayama discloses that the power distributing circuit (12 and 13) is inherently a high-power resistor having a capability to handle power higher than the allowable power of the driving device in order to regulate the high voltage from the AC source to the transistors (6, 7, 8) of the driving device (5).

Regarding Claim 19, Katayama discloses that the power distributing circuit (12 & 13) is a resistive element having an impedance whose value is inherently not small than 1/10 of the value of a resistive component of the conducting impedance of the driving device (5) divided by the number of driving devices since the resistors (12 and 13) must be particularly high in order to regulate the high voltage from the AC source (9) and the resistive component inside the transistors (6, 7, 8) of driving device (5) are driven with small gate current (See Col. 4, lines 10-13) and 1/10 of the value of the resistive component in the driving device is intended to be very small.

Regarding Claim 20, Katayama discloses that the power distributing circuit (12 and 13) is inherently a high-power resistor having a capability to handle power higher than the allowable power of the driving device in order to regulate the high voltage from the AC source to the transistors (6, 7, 8) of the driving device (5).

Regarding Claim 35, Katayama discloses a capacitive load driving circuit for driving a capacitive load (4), connected to an output terminal (5a), by a driving device (5), comprising a resistive impedance (12 and 13) inserted in series to the output terminal (5a) (See Figure 3).

In addition, Katayama discloses that the power distributing circuit (12 and 13) is a resistive element having an impedance whose value is inherently not small than 1/10 or 3/10 of the value of a resistive component of the conducting impedance of the driving device (5) since the resistors (12 and 13) must be particularly high in order to regulate the high voltage from the AC source (9) and the resistive component inside the transistors (6, 7, 8) of driving device (5) are driven with small gate current (See Col. 4, lines 10-13) and 1/10 or 3/10 of the value of the resistive component in the driving device is intended to be very small.

Regarding Claim 37, Katayama discloses that the power distributing circuit (12 and 13) is a resistive element having an impedance whose value is inherently not small than 1/10 or 3/10 of the value of a resistive component of the conducting impedance of the driving device (5) since the resistors (12 and 13) must be particularly high in order to regulate the high voltage from the AC source (9) and the resistive component inside the transistors (6, 7, 8) of driving device (5) are driven with small gate current (See Col. 4,

lines 10-13) and 1/10 or 3/10 of the value of the resistive component in the driving device is intended to be very small.

Alternately, it would have been to one of ordinary skill in the art to tune any appropriate resistance value in Katayama in order to attain a desired output. Besides, it is also held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).* And it is not inventive to discover the optimum or workable ranges by routine experimentation merely involves routine skill in the art. *In re Aller*, 220 F. 2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding Claim 38, Katayama discloses that a driving power supply source (9) connected to the output terminal (5a) via the driving device (5); and a power distributing circuit (12 and 13) inserted between the driving power supply source (9) and the driving device (5) (See Figure 3).

Regarding Claim 39, Katayama discloses that a reference potential point (terminals +, -) of the power source (9) connected to the output terminal (5a) via the driving device (5); and a power distributing circuit (12 and 13) inserted between the reference potential point (+, -) and the driving device (5).

Regarding Claim 40, Katayama discloses that a plurality of driving devices (6) for driving a plurality of capacitive loads (4), formed in integrated-circuit form (See abstract), wherein each of the driving devices is connected to a driving power supply source (9) or a reference potential point (terminals +, -) via a power distributing circuit (12 and 13) (See Figure 3).

Regarding Claims 87, 90, 93 and 96, Katayama discloses that the capacitive-load driving circuit is used as an electrode driving circuit of a plasma display apparatus to drive address electrodes thereof (scanning electrodes) (See Col. 1, lines 35-67 and Col. 3, lines 7-35). Besides, using his invention in any apparatus such as plasma display apparatus is considered as an intended use.

Allowable subject matter

Claims 30, 31, 72, 84, 85, 88, 89, 91, 92, 94, 95, 97 and 98 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 33, 63, 64 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art fails to disclose the followings:

- The driving power supply source raises or lowers an output voltage is steps by switching the output voltage between the plurality of voltage levels within a driving voltage amplitude, while retaining On/OFF states of the driving devices such as required by claim 33.
- A flip flop that drives a control input of the output device to a full-swing level either at the driving power supply voltage or at the reference potential such as required by claim 63.
- Each of the driving integrated circuits includes a buffer driven by a logic voltage, and an output of the buffer is connected to an input terminal of each

driving device, and power distributing circuit is connected to an inverting input terminal of each driving device, and supplying self-biasing to the driving to the driving device by a voltage drop occurring across the power distributing circuit such as required by claim 64.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

This application contains claims 41-62 drawn to an invention nonelected without traverse in Paper No. 5. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Wilson Lee whose telephone number is (703) 306-3426.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center receptionist whose telephone number is (703) 308-0956.

Papers related to Technology Center 2800 applications may be submitted to Technology Center 2800 by facsimile transmission. Any transmission not to be considered an official response must be clearly marked "DRAFT". The Technology Center Fax Center number is (703) 308-7722 or (703) 308-7724.

WL
11/17/03

Don Wong
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Technology Center 2800